



Express Mail No. EV060042762US
Atty. Dkt. No. 037267-0135

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Takaaki NAGAI et al.
Title: EEPROM SEMICONDUCTOR
DEVICE AND METHOD OF
FABRICATING THE SAME
Appl. No.: 09/606,159
Filing Date: 06/29/2000
Examiner: P. Brock, II
Art Unit: 2815

CERTIFICATE OF EXPRESS MAILING	
I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: Commissioner for Patents, Washington, D.C. 20231.	
EV060042762US	December 4, 2002
(Express Mail Label Number)	(Date of Deposit)
Beatriz Valencia	
(Printed Name)	
<i>Beatriz Valencia</i>	
(Signature)	

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TECHNOLOGY CENTER 2800
DEC -9 2002

AMENDMENT TRANSMITTAL

Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

- ☐ Small Entity status under 37 C.F.R. § 1.9 and § 1.27 has been established by a Small Entity statement previously submitted.
- ☐ Small Entity statement is enclosed.
- ☒ The fee required for additional claims is calculated below:

	Claims as Amended		Previously Paid For		Extra Claims Present		Rate		Additional Claims Fee
Total Claims:	6	—	20	=	0	x	\$18.00	=	\$0.00
Independents:	2	—	3	=	0	x	\$84.00	=	\$0.00
First presentation of any Multiple Dependent Claims:						+	\$280.00	=	\$0.00
CLAIMS FEE TOTAL:									\$0.00

- ☒ Applicant hereby petitions for an extension of time under 37 C.F.R. § 1.136(a) for the total number of months checked below:

<input type="checkbox"/>	Extension for response filed within the first month:	\$110.00	\$0.00
<input type="checkbox"/>	Extension for response filed within the second month:	\$400.00	\$0.00
<input checked="" type="checkbox"/>	Extension for response filed within the third month:	\$920.00	\$920.00
<input type="checkbox"/>	Extension for response filed within the fourth month:	\$1,440.00	\$0.00
<input type="checkbox"/>	Extension for response filed within the fifth month:	\$1,960.00	\$0.00
EXTENSION FEE TOTAL:			\$920.00
CLAIMS AND EXTENSION FEE TOTAL:			\$920.00
<input type="checkbox"/>	Small Entity Fees Apply (subtract ½ of above):		\$0.00
TOTAL FEE:			\$920.00

- ☐ Please charge Deposit Account No. 19-0741 in the amount of \$920.00. A duplicate copy of this transmittal is enclosed.
- ☒ A check in the amount of \$920.00 is enclosed.
- ☒ The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,

Date 12-4-02

By Richard D. Malone

FOLEY & LARDNER
Customer Number: 22428

Richard D. Malone
Attorney for Applicant
Registration No. 51,991



22428

PATENT TRADEMARK OFFICE

Telephone: (310) 975-7895
Facsimile: (202) 672-5399



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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 Title: EEPROM SEMICONDUCTOR
 DEVICE AND METHOD OF
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#810

Amend

Jim Miller

1/7/03

Appl. No.: 09/606,159

Filing Date: 06/29/2000

Examiner: P. Brock, II

Art Unit: 2815

AMENDMENT AND REQUEST FOR
 RECONSIDERATION UNDER 37 C.F.R. § 1.111

Commissioner for Patents
 Washington, D.C. 20231

Sir:

In response to the Office Action mailed June 5, 2001, time for response to which is extended three months (to December 5, 2002) by the accompanying petition, please amend the above-identified application as follows:

IN THE CLAIMS:

Please enter the following amended claims:

21. (Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising the steps of:
- (a) forming a plurality of field insulating films in parallel with one another on a semiconductor substrate;
 - (b) forming a first gate insulating film in each of active regions;
 - (c) forming a plurality of first polysilicon strips in parallel with one another;
 - (d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

sub E1
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